minIC™

Arm® Cortex®-M0+ 32-bit Microcontroller

192 KB SRAM · 80 MHz † · 12-bit ADC · Single 3.3 V supply

HEX MICROCHIP

PRELIMINARY

Work in progress · Rev 1.2

minIC is a general-purpose 32-bit microcontroller built around an Arm Cortex-M0+ core, combining a broad mixed-signal peripheral set — CAN, LIN, quad-lane xSPI, a 12-bit SAR ADC and a hardware PID accelerator alongside four PWM channels. The application is held in SPI NOR flash and run from SRAM. It targets appliance, industrial, automotive and building-control applications from a single 3.3 V supply.

KEY FEATURES

Processor

- Arm® Cortex®-M0+, ARMv6-M, little-endian
- 9-cycle interrupt latency · 4 priority levels
- 32-channel NVIC · 24-bit SysTick timer
- Single-master AHB-Lite interconnect

Memory

- 16 KB boot ROM
- 192 KB SRAM in two banks (128 KB + 64 KB)
- SPI NOR flash interface, up to 16 MB, on dedicated pads
  - Holds the application image, parameters and data in one device
  - Can be co-packaged with the die as a system in package
- Application copied to SRAM at boot and executed from there
  - Leaves the flash interface free for parameters and data
  - Execute-in-place from the flash window also supported

Clocks & Reset

- 80 MHz PLL with automatic frequency calibration †
- Tunable 4–12 MHz HSI RC oscillator †
  - Coarse and fine trim, power-down control
- Always-on 30 kHz LSI RC oscillator †
- External crystal or reference clock, 2–48 MHz
- Glitch-free 5-input system clock multiplexer
  - Boot clock selectable by external pin
- Independent RTC clock and reset domain
- Low-speed clock monitor with threshold interrupt

Connectivity

- 2× UART with LIN 2.x and IrDA, up to 10 Mbaud †
  - 32-byte FIFOs, 16-entry LIN frame-ID table, master or slave node
- 1× UART, basic, up to 5 Mbaud †
- 3× I²C master, 100 kHz and 400 kHz fast mode
- 2× SPI/SSP, master or slave, 8-entry FIFOs
- 1× xSPI (extended SPI) master, up to 40 MHz †
  - Single-lane SPI, dual-lane DSPI and quad-lane QSPI modes
- 1× CAN 2.0A/B, 25 kbit/s to 1 Mbit/s

Control & Timing

- PID accelerator, Q1.15 gains, Q17.15 output
- 4-channel PWM, glitch-free shadow commit
- 4× 32-bit timer counter
- RTC with two alarms and event time-stamp

Analog & Power

- 12-bit SAR ADC, 8 external plus 7 internal channels
  - Rail-to-rail input range at 3.3 V
  - Internal channels: temperature, bandgap, DAC output, core supply, common mode and both conversion references
- 17-bit signed ΔΣ DAC (±65535 codes about midscale)
  - Up to 100 kSa/s update rate, suitable for audio with an external filter and driver
- Analog comparator with edge-triggered interrupt
  - Both inputs independently selectable from two external pins, DAC output, temperature, bandgap, and the core and I/O supplies
- 1.2 V bandgap voltage reference
- On-chip LDO regulator with ready status
- Power-on reset and brown-out detect, 4 selectable levels

I/O & Debug

- 32 GPIO with alternate and analog function select
  - Per-pin interrupt, drive strength and pull-up control
- JTAG debug port, 4 breakpoints and 2 watchpoints

† *Clock frequencies and the interface rates derived from them are targets, pending silicon characterization.*

QUICK SPECIFICATIONS

Summary of all integrated peripherals and system characteristics.

CORE & SYSTEM

Processor	**Cortex-M0+**
Architecture	**ARMv6-M**
Max system clock	**80 MHz †**
Interrupt controller	**NVIC, 32 lines**
System bus	**AHB-Lite**
Endianness	**Little-endian**

MEMORY

SRAM	**192 KB**
SRAM organization	**128 KB + 64 KB**
Boot ROM	**16 KB**
SPI NOR flash	**Up to 16 MB**
Flash interface	**Single-lane, dedicated pads**
Flash write access	**Via xSPI**

CLOCKS & RESET

PLL / VCO	**80 MHz †**
HSI oscillator	**4 – 12 MHz, tunable †**
LSI oscillator	**30 kHz †**
External reference	**2 – 48 MHz**
System clock sources	**5, glitch-free**
Clock monitor	**1**

COMMUNICATION

UART with LIN / IrDA	**2, ≤ 10 Mbaud †**
UART, basic	**1, ≤ 5 Mbaud †**
I²C master	**3, 100 / 400 kHz**
SSP / SPI	**2**
xSPI master (SPI/DSPI/QSPI)	**1, ≤ 40 MHz †**
CAN 2.0A/B	**1, 25 kbit/s – 1 Mbit/s**
LIN frame-ID table	**16 entries**

TIMERS & CONTROL

32-bit timer counters	**4**
PWM channels	**4**
PID accelerator	**1**
Real-time clock	**1 (2 alarms)**
SysTick timer	**24-bit**

ANALOG

ADC resolution	**12-bit SAR**
ADC channels	**8 external + 7 internal**
ADC input range	**Rail-to-rail**
DAC resolution	**17-bit signed**
DAC code range	**±65535, midscale**
DAC update rate	**≤ 100 kSa/s**
DAC output stage	**External filter / driver**
Analog comparator	**1, with interrupt**
Comparator inputs	**7 sources per input**
Temperature sensor	**Via ADC channel**

POWER

I/O supply (VDDIO)	**3.3 V (3.0 – 3.6)**
Core supply	**On-chip LDO**
Voltage reference	**Bandgap, 1.2 V**
Power-on reset	**Integrated**
Brown-out detect	**4 levels, interrupt**
Reset sources	**External / POR / SW**

I/O, DEBUG & TEST

GPIO pins	**32**
GPIO interrupts	**Per-pin, level/edge**
Debug interface	**JTAG**
Test mode	**Analog test SPI**
Package options	**QFN64 / 80 / 88 / 100**
Package, final	**TBD**

† Target values, pending silicon characterization. Interface rates scale with the system clock.

SYSTEM BLOCK DIAGRAM

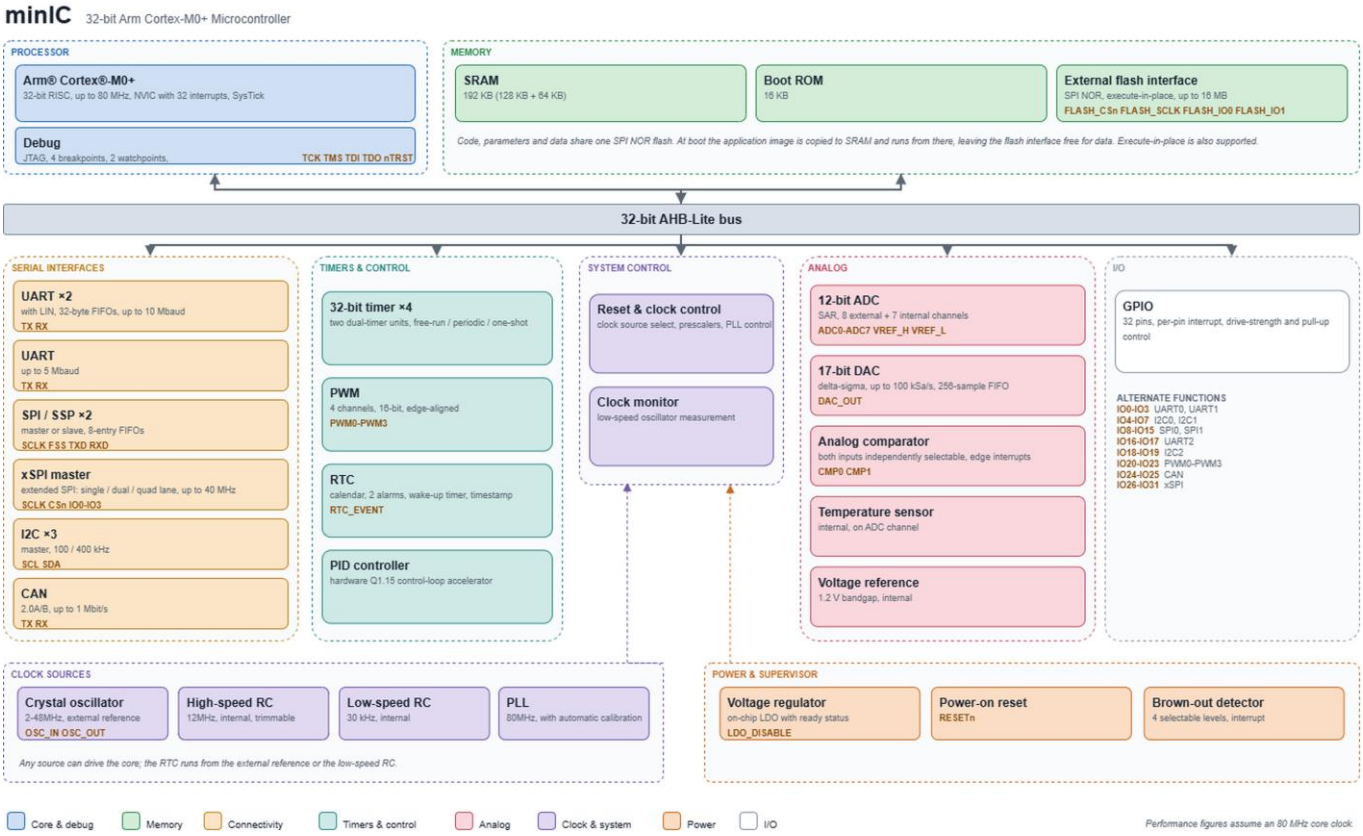


Figure 1. minIC system block diagram. Performance figures assume an 80 MHz core clock. Per-block IP ownership is listed on page 5.

CUSTOM VARIANTS

minIC is a platform rather than a fixed product. The directions below can be developed for a specific programme — contact HEX Microchip to discuss requirements.

SecureIoT

Hardware AES, SHA and public-key acceleration with a true random number generator, secure boot and key storage, targeting PSA Certified and SESIP evaluation.

Encrypted code execution

On-the-fly decryption of the flash interface, so the application image is never exposed in plain text on the board.

Edge AI acceleration

A neural-network accelerator for keyword spotting, anomaly detection and predictive maintenance, with the on-chip SRAM holding the model.

Higher-performance core and interfaces

A Cortex-M33 core with TrustZone and DSP extensions, together with modern interfaces such as I3C, USB and single-pair Ethernet.

Functional safety

ISO 26262 and IEC 61508 development, with lockstep execution, SRAM error correction and built-in self-test.

Automotive qualification

AEC-Q100 qualification and extended temperature range, with CAN FD and CAN XL alongside the LIN interfaces already integrated.

Enhanced analog front end

Higher-resolution sigma-delta conversion, programmable-gain amplifiers and on-chip operational amplifiers for precision sensing.

Ultra-low power

Deep-sleep modes with RTC retention and wake-on-event, for battery and energy-harvesting designs.

TYPICAL APPLICATION

Appliance controller. Every interface shown is integrated in minIC; the external components are application-specific.

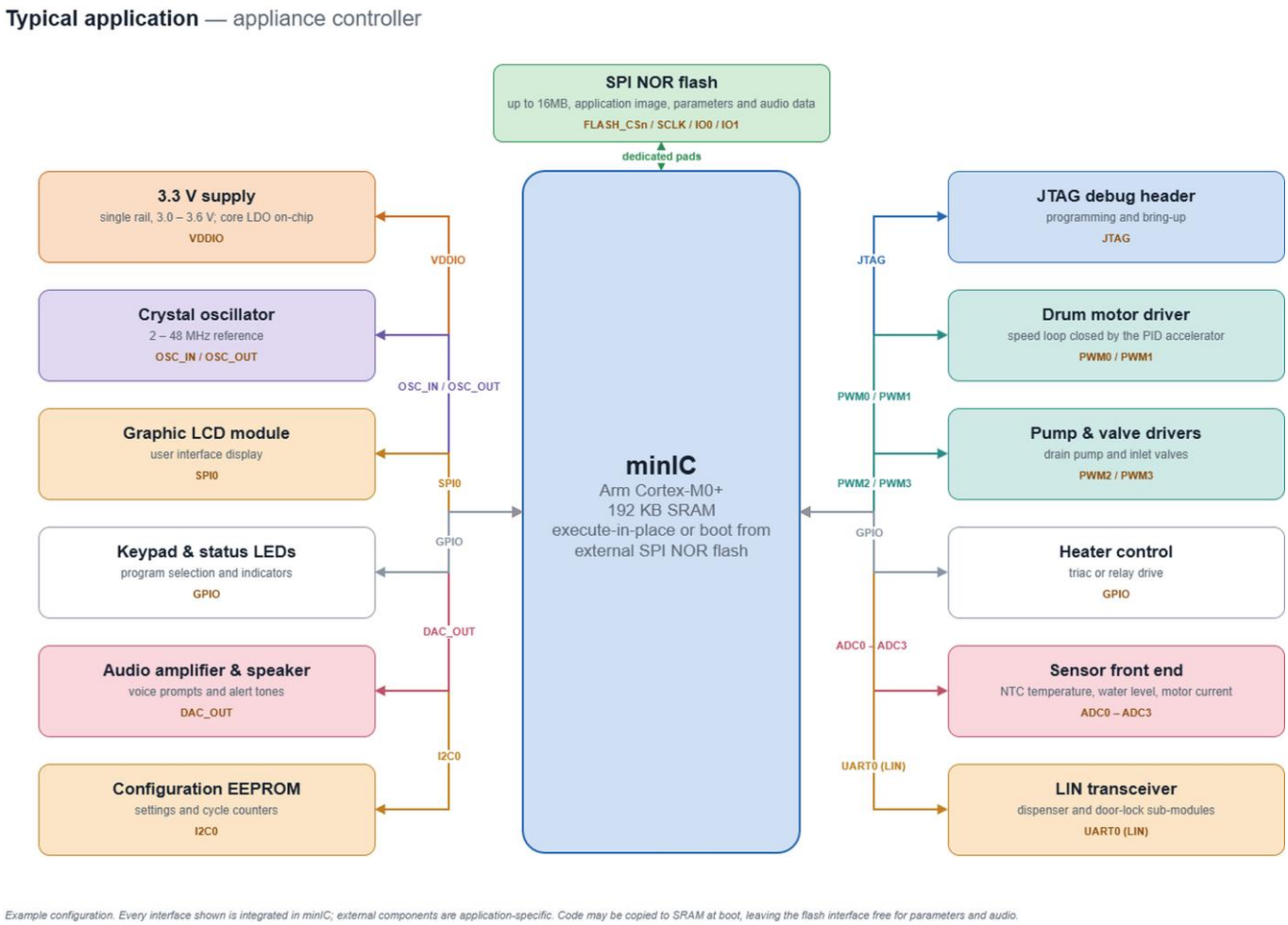


Figure 2. One SPI NOR flash holds the application image, parameters and audio data. The application may run in place or be copied to SRAM at boot.

TARGET APPLICATIONS

Appliances

Washers, dishwashers, ovens and small domestic appliances: motor, heater and panel control with voice prompts

Industrial

Factory automation, PLC I/O modules, sensor and actuator interfaces, closed-loop process control

Automotive

Body electronics, LIN sub-networks, LIN/CAN gateways, comfort, lighting and mirror control

Building & HVAC

Thermostats and zone controllers, valve and damper actuators, air handling, environmental sensing

Energy & Metering

Battery management, current sensing, power conversion control, sub-metering and monitoring

Motor & Drives

Brushed DC and stepper drive, pumps, fans and compressors, speed and position loops

PERIPHERAL REFERENCE

Detailed capability summary for each integrated block.

Group	Peripheral	Qty	IP	Key specifications
Core	Arm Cortex-M0+	1	Arm	ARMv6-M, r0p1 · Thumb®/Thumb-2 · little-endian · 9-cycle IRQ latency · 32 NVIC lines, 4 priority levels
Memory	SRAM	192 KB	TSMC	128 KB + 64 KB banks · twelve 16 KB single-port macros · AHB multi-bank controller
	Boot ROM	16 KB	HEX	Read-only · holds the boot image and vector table
	SPI NOR flash interface	1	HEX	Up to 16 MB on dedicated pads, independent of the GPIO mux · holds the application image, parameters and data · memory-mapped execute-in-place read also supported · can be co-packaged as a system in package
Clocks	PLL	1	HEX	80 MHz VCO · automatic frequency calibration and bring-up sequencing †
	HSI RC oscillator	1	HEX	4 – 12 MHz, tunable · coarse and fine trim · power-down control †
	LSI RC oscillator	1	HEX	30 kHz, always-on · clocks the RTC domain reset †
	Clock monitor	1	HEX	LSI period deviation, jitter and history capture · programmable threshold interrupt
	Clock & reset manager	1	HEX	Five-source glitch-free system multiplexer · independent RTC mux · per-domain reset control
Power	Core LDO	1	HEX	Single VDDIO supply (3.0–3.6 V) feeds the I/O ring; on-chip LDO derives the core voltage
	Bandgap & bias	1	HEX	1.2 V reference · PTAT bias generator · disable input
	POR & brown-out detect	1	HEX	Power-on reset · brown-out detection with four selectable levels and its own interrupt
Comm	UART with LIN / IrDA	2	HEX	UART, IrDA and LIN modes · up to 10 Mbaud †, and 20 Mbaud at the cost of an increased bit error rate · 32-byte TX/RX FIFOs · hardware PID parity and checksum · 16-entry frame-ID table · master or slave node
	UART, basic	1	Arm *	Programmable baud divider, up to CLK/16, i.e. 5 Mbaud at 80 MHz † · TX/RX buffers · separate TX, RX and overrun interrupts
	I²C master	3	HEX • OC *	100 kHz standard mode and 400 kHz fast mode · multi-master arbitration · clock stretching · open-drain via the GPIO mux
	SSP / SPI	2	Arm *	Master or slave · SPI, TI SSI and Microwire frame formats · 4–16 bit data · TX/RX FIFOs
	xSPI master	1	HEX	Extended SPI (HEX naming), covering single-lane SPI, dual-lane DSPI and quad-lane QSPI · SCLK up to CLK/2, i.e. 40 MHz at 80 MHz † · 256-byte FIFOs · programmable command, dummy and CS timing · in-system flasher mode
	CAN 2.0A/B	1	HEX • OC *	1 Mbit/s maximum, configurable down to 25 kbit/s at 80 MHz † · BasicCAN and PeliCAN modes · acceptance filter · programmable bit timing
Timers	32-bit timer counter	4	Arm *	Two dual-timer modules · 16- or 32-bit operation · programmable prescaler · free-running, periodic and one-shot
	Real-time clock	1	HEX	Independent clock and reset domain · calendar with ISO 8601 day-of-week · two alarms · periodic wakeup · event time-stamp · digital calibration
Control	PWM	4 ch	HEX	Edge-aligned · per-channel divider, period and duty · glitch-free shadow commit · programmable idle level · per-channel pad output enable
	PID accelerator	1	HEX	Q1.15 gains, set-point and process variable · Q17.15 output · output saturation with conditional-integration anti-windup
Analog	SAR ADC	1	HEX	12-bit · 8 external channels plus 7 internal: temperature sensor, bandgap reference, DAC output, core supply, common mode and both conversion references · per-channel averaging · rail-to-rail input at 3.3 V · detailed specifications pending characterization
	ΔΣ DAC	1	HEX	Second-order modulator, 17-bit signed code (±65535 about midscale) · V_OUT = V_midscale + (code / 65535) × (V_FS_span / 2), with LSB = V_FS_span / 131070 · up to 100 kSa/s update rate · usable for audio output with an external reconstruction filter and driver · 256-sample FIFO
	Analog comparator	1	HEX	Positive and negative inputs independently selectable from seven sources each: two external channels, the DAC output, the temperature sensor, the bandgap reference, the I/O supply and the core supply · edge-triggered interrupt · detailed specifications pending characterization
I/O	GPIO	32	HEX	Per-pin alternate and analog function select · per-pin interrupt, level or edge, either polarity · atomic set and clear · per-pin input enable, pull and drive strength
Debug	JTAG debug port	1	Arm	CoreSight debug access port with system ROM table
	Analog test (DFT)	1	HEX	SPI access for analog bring-up and production test

** Planned for replacement with HEX in-house IP in a future revision.* *† Target values, pending silicon characterization. Interface rates scale with the system clock.*

For complete register maps, memory map and electrical characteristics, refer to the minIC datasheet.

Preliminary document. This device is under active development; all specifications are subject to change without notice.

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